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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,021	07/17/2003	Alexander C. Klaiber	TRAN-P076	4477

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,021	KLAIBER ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *17-19* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action responsive to communication filed May 13, 2004. Claims 1-16 and 20-28 are presented for examination. Claims 17-19 have been withdrawn from examination due to the non-elected group of claims.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

NOTIFICATION OF OBJECTION AND/OR REJECTIONS

Election of Species/Restriction

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-16 and 20-28 drawn to a system and method for enforcing a consistent cacheability attribute for a page of physical memory through a utilization of a translation lookaside buffer, classified under class 711 subclass 205.

Group II. Claims 17-19, drawn specifically to a data structure disposed in a computer readable memory for providing information corresponding to a current cacheability characteristic attributed to a page of physical memory, classified in class 711 subclass 209.

The inventions are distinct, each from the other for the

following reasons:

The invention of groups I and II are related as combination/subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, the invention of group I has separate utility such as a method and system for maintaining data coherency in a system having a translation lookaside buffer and is not limited for use or implemented with a data structure disposed in a computer readable memory for providing information corresponding to a current cacheability characteristic attributed to a page of physical memory according group II. Similarly, the system of group II can be implemented as a memory storage device or data structure utilized in a network environment for page address indexing, and is not restricted for use with system and method for enforcing a consistent cacheability attribute for a page of physical memory through a utilization of a translation lookaside buffer of group I. See M.P.E.P. § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and recognized divergent subject matter, and because the search required for one group is not coextensive with the search required for the other groups, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. Lawrence R. Goerke (Reg. No. 45,927) on August 19, 2005; a provisional election was made without traverse to prosecute the invention of group I, claims 1-16 and 20-28. Claims 17-19 are therefore withdrawn from further consideration by the Examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 C.F.R. § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 C.F.R. § 1.48(b) and by the fee required under 37 C.F.R. § 1.17(i).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4, 8, 10-12, 16 and 20-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Pedneau (USPN: 6,189,074).

As per claim 1, Pedneau discloses the invention as claimed including a computer implemented method for enforcing a consistent cacheability attribute for a page of physical memory, comprising (e.g. see abstract) storing a current cacheability characteristic attributed to a physical address of said page of physical memory (e.g. see col. 4, lines 30-31); accessing an identifier of said page of physical memory and an associated desired cacheability state corresponding to said physical memory page from a candidate entry to a translation lookaside buffer (e.g. see col. 4, lines 50-57), comparing said current cacheability characteristic and said desired cacheability state (e.g. see col. 4, lines 57-58); upon a match, entering said candidate entry to said translation lookaside buffer (e.g. see col. 4, lines 64-66); and upon a mismatch, generating an exception wherein said exception causes enforcement of said consistent cacheability charaderistic is taught by Pedneau as when mismatch occurs (e.g. present bit in the table entry is 0), the processor will generate a page fault, wherein the data will swap from disk to enforce the coherence of the cacheability characteristic (e.g. see col. 4, lines 15 et seq.);

As per claim 2, wherein said storing, accessing, and comparing are performed upon receiving said candidate entry to said translation lookaside buffer is taught by Peneau since all the transactions are being performed with respect to transaction

loaded in a translation lookaside buffer reload operation (e.g. see abstract, column 4, lines 25-30).

As per claim 3, Pedneau discloses mapping the physical address of the page of physical memory to a table as being equivalent to logical address being translated into linear address which is then further translated into physical address thru mapping to the translation table wherein the physical address is used to determine the cacheability characteristic of the page of the physical memory (e.g. see col. 1, lines 41-54; column 4, lines 30 et seq.);

As per claim 4, Pedneau discloses generating an exception comprises conforming the current cacheability characteristic to the desired cacheability state as being equivalent to in response to the linear address miss in the translation lookaside buffer, the processor is configured to locate a translation corresponding to the linear address within a plurality of page tables in the main memory and storing the second page frame based address and the second cacheability indicator in one of the plurality of translation entries (e.g. see column 10, lines 39-55);

As per claim 8, Pedneau disclose walking/searching a page table having a plurality of page table entries as being equivalent to comparing/walking all entries in the translation lookaside buffer 55 to the linear address using a virtual

address to find a page table entry corresponding to the physical memory page (e.g. see col. 8, lines 5-8); extracting the page table entry corresponding to the physical memory page when TLB HIT (e.g. see col. 8, lines 9 et seq.); and determining the physical page identifier and the desired cacheability state from the page table entry (e.g. see column 8, lines 11-14);

As per claims 9-12 and 16, they encompass the same scope of invention as to that of claims 1-4 and 8, the claims are therefore rejected for the same reasons as being set forth above. It's noted that the second cacheability bit from a table which is utilized during the comparison transaction is embedded in the system of Pedneau since Peneau clearly discloses multiple cacheability attributes are being utilized (e.g. see column 4, lines 57-58; column 7, lines 53-56);

As per claims 20 and 23, Pedneau discloses a computer based system for enforcing a consistent cacheability attribute for a page of physical memory upon entry of said page into a translation lookaside buffer (e.g. see abstract) comprising a comparator 1007 (e.g. figure 8) for comparing an current cacheability characteristic attributed to said page of physical memory and a desired cacheability state for said page (e.g. see column 6, lines 22 et seq.), wherein comparator 1007 is coupled to the translation lookaside buffer 1009 (e.g. see figure 8); miss handler is equivalently taught as a memory management unit

(not shown but detailed by Pedneau; e.g. see column 6, lines 14 et seq.) coupled to comparator 1007 and to the translation lookaside buffer 1009 for handling a miss in the translation lookaside buffer 1009 upon the comparator 1007 determining that the current cacheability characteristic and the desired cacheability state match (also see column 6, lines 57-60); and an exception handler (also part of the memory management unit, not shown but detailed by Pedneau, e.g. see column 6, lines 14 et seq.) coupled to the comparator 1007 and to the translation lookaside buffer 1009 for handling an exception generated by comparator 1007 upon the comparator determining that the current cacheability characteristic and the desired cacheability state do not match (or miss) (e.g. see column 6, lines 58-60; also see column 8, lines 22 et seq.).

As per claim 21, Pedneau discloses a page table entry walker-extractor as a translation control unit 54 coupled to translation lookaside buffer 1009 for accessing a page table entry in a physical memory, walking said page table entry, locating an appropriate page table entry, and extracting said appropriate page table entry for said translation lookaside buffer (e.g. see column 8, lines 5 et seq.);

As per claim 22, Pedneau discloses the system is deployed within a processor or processing unit 1002 (e.g. see figure 8, lines 10 et seq.);

As per claim 24, Pedneau discloses the cacheability mode transition comprises a transition from cacheable to non-cacheable as being equivalent to the transition of PCD bit from 0 to 1 (inherent in the system of Pedneau to indicate cacheability mode from cacheable to non-cacheable or vice versa (e.g. see column 7, lines 35-41); removing an old entry with the address from said translation lookaside buffer is equivalent taught by Pedneau as a LRU replacement mechanism wherein old entry is replaced with the new data entry (e.g. see column 3, lines 32 et seq.); updating said current cacheability characteristic to non-cacheable; flushing a cache of a page corresponding to said address, and entering said candidate entry to said translation lookaside buffer (e.g. see column 9, lines 6-15);

As per claim 25, wherein said cacheability mode transition comprises a transition from non-cacheable to cacheable as being equivalent to the transition of PCD bit from 0 to 1 (inherent in the system of Pedneau to indicate cacheability mode from cacheable to non-cacheable or vice versa (e.g. see column 7, lines 35-41); and wherein the correcting comprises draining a pending write (write gathering) from a non-cacheable path (e.g. see column 7, lines 26-49); removing an old entry with said physical page identifier from said translation lookaside buffer as being equivalently taught by Pedneau as a

LRU replacement algorithm (e.g. see column 3, lines 32 et seq.) ; updating the current cacheability characteristic to cacheable; and entering said candidate entry to said translation lookaside buffer (e.g. see column 9, lines 6-15).

Allowable subject matter

8. Claims 5, 13 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. The prior arts of record do not teach nor suggest determining a cacheability transition to conform the current cacheability characteristic to the desired cacheability state; determining a conservatism character of a mode of execution, upon determining that said conservatism character is aggressive: rolling back to the last commit point in the execution; changing said conservatism character to conservative, wherein the changing comprises disallowing speculation, and repeating said execution without speculation until said exception is reached, upon determining that said cacheability transition comprises a cacheable to non-cacheable transition, performing said cacheable to non-cacheable transition, and upon determining that said cacheability transition comprises a non-cacheable to cacheable transition, performing said non-cacheable to cacheable transition as being claimed. Claims 6-7, 14-15 and 27-28 are also allowable since

they are depended upon the indicated allowable claims 5 and 13 respectively.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/August 20, 2005

Tuan V. Thai
PRIMARY EXAMINER
Group 2100